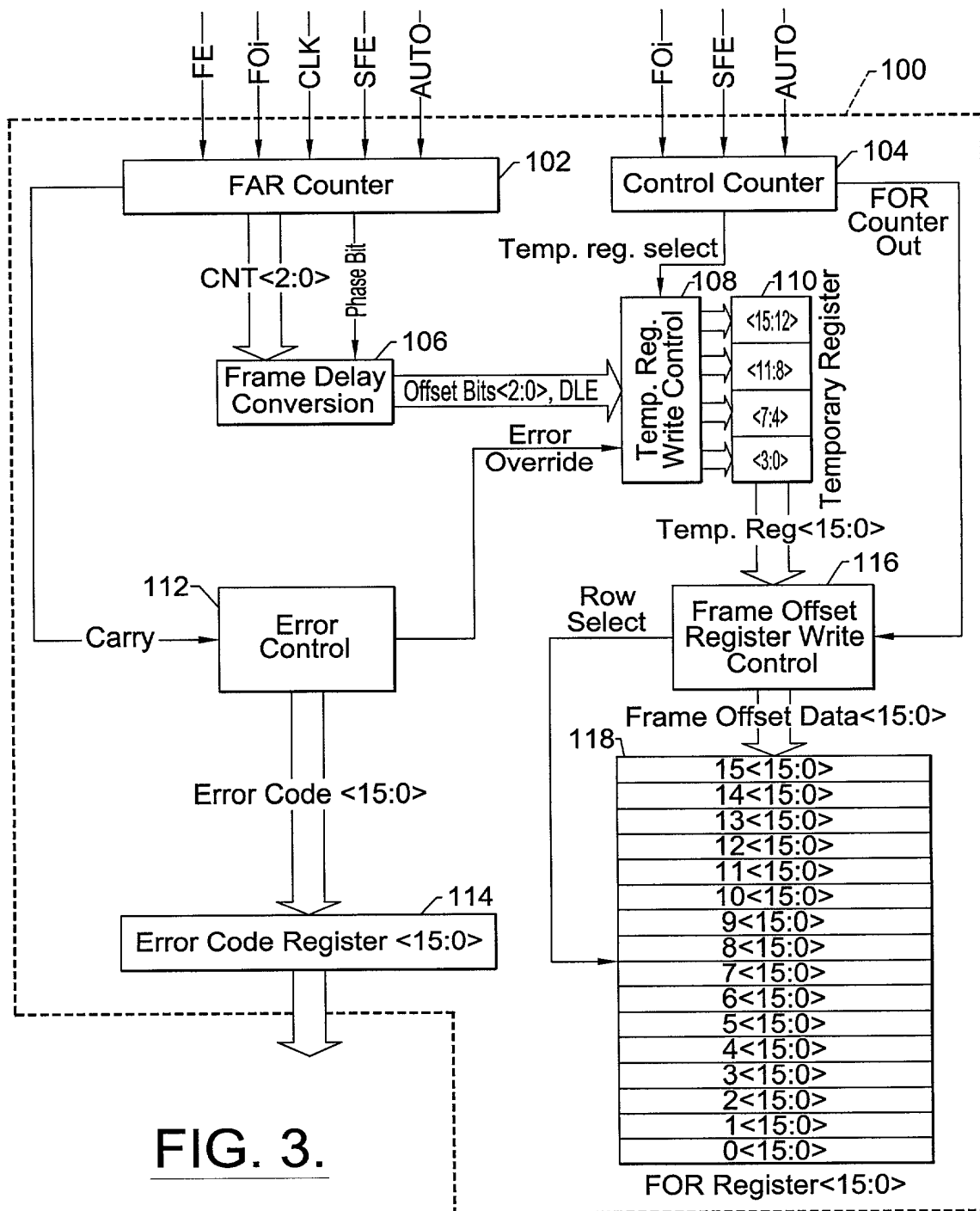


**FIG. 1.**  
(PRIOR ART)

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Offset Bits			
	FD11	FD2	FD1	FD0	OFn2	OFn1	OFn0	DLEn
No clock period shift (Default)	1	0	0	0	0	0	0	0
+0.5 clock period shift	0	0	0	0	0	0	0	1
+1.0 clock period shift	1	0	0	1	0	0	1	0
+1.5 clock period shift	0	0	0	1	0	0	1	1
+2.0 clock period shift	1	0	1	0	0	1	0	0
+2.5 clock period shift	0	0	1	0	0	1	0	1
+3.0 clock period shift	1	0	1	1	0	1	1	0
+3.5 clock period shift	0	0	1	1	0	1	1	1
+4.0 clock period shift	1	1	0	0	1	0	0	0
+4.5 clock period shift (max)	0	1	0	0	1	0	0	1

FIG. 2.

(PRIOR ART)



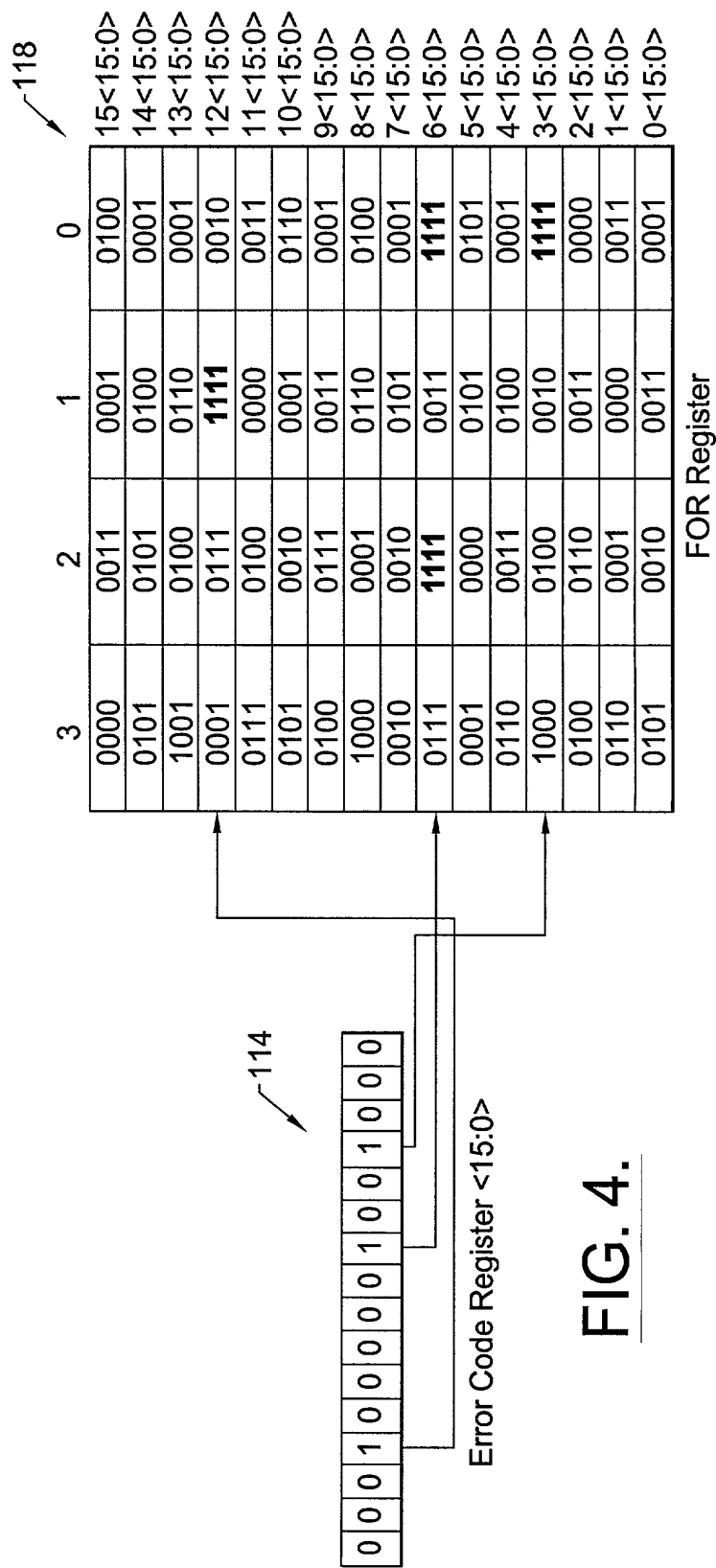
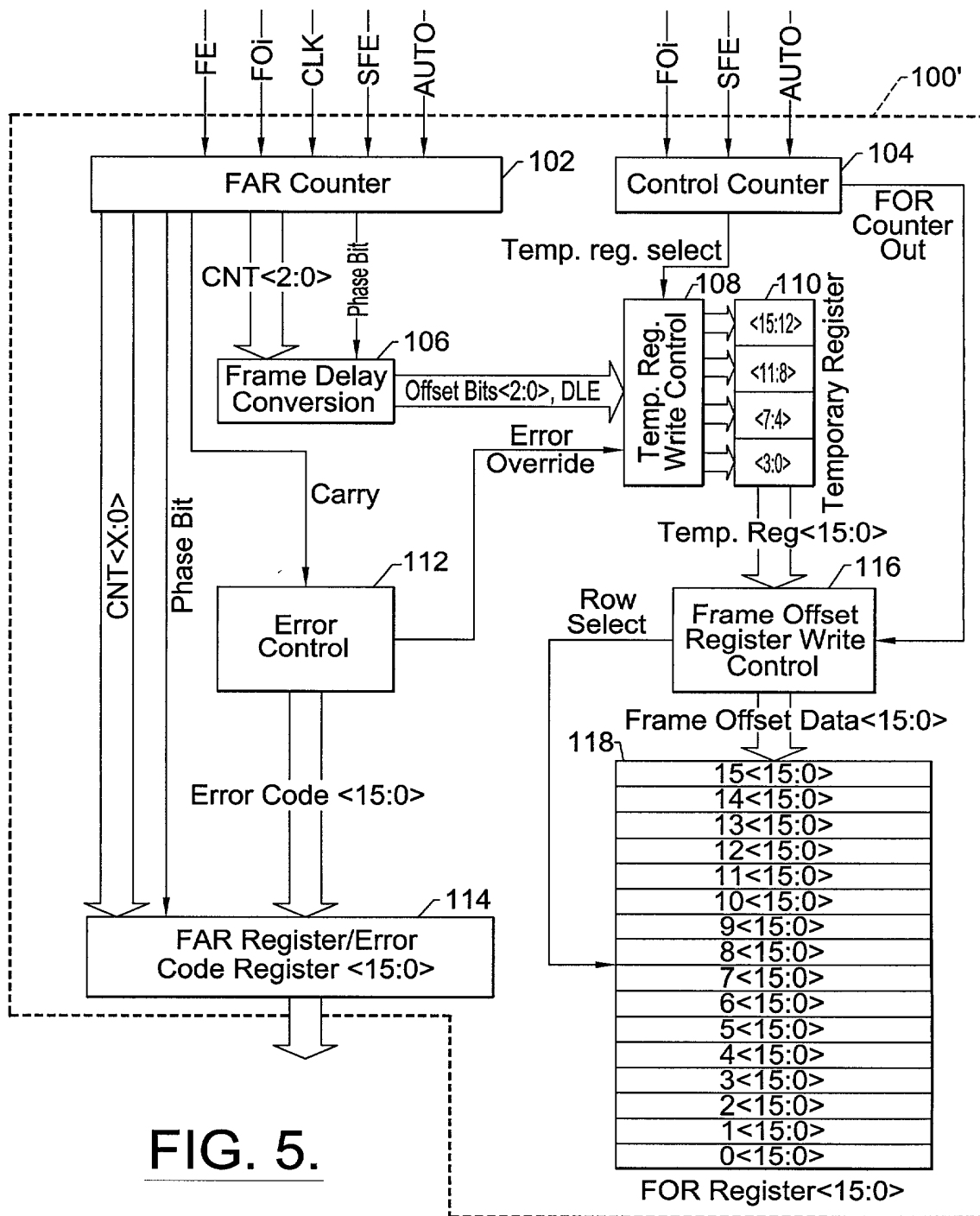
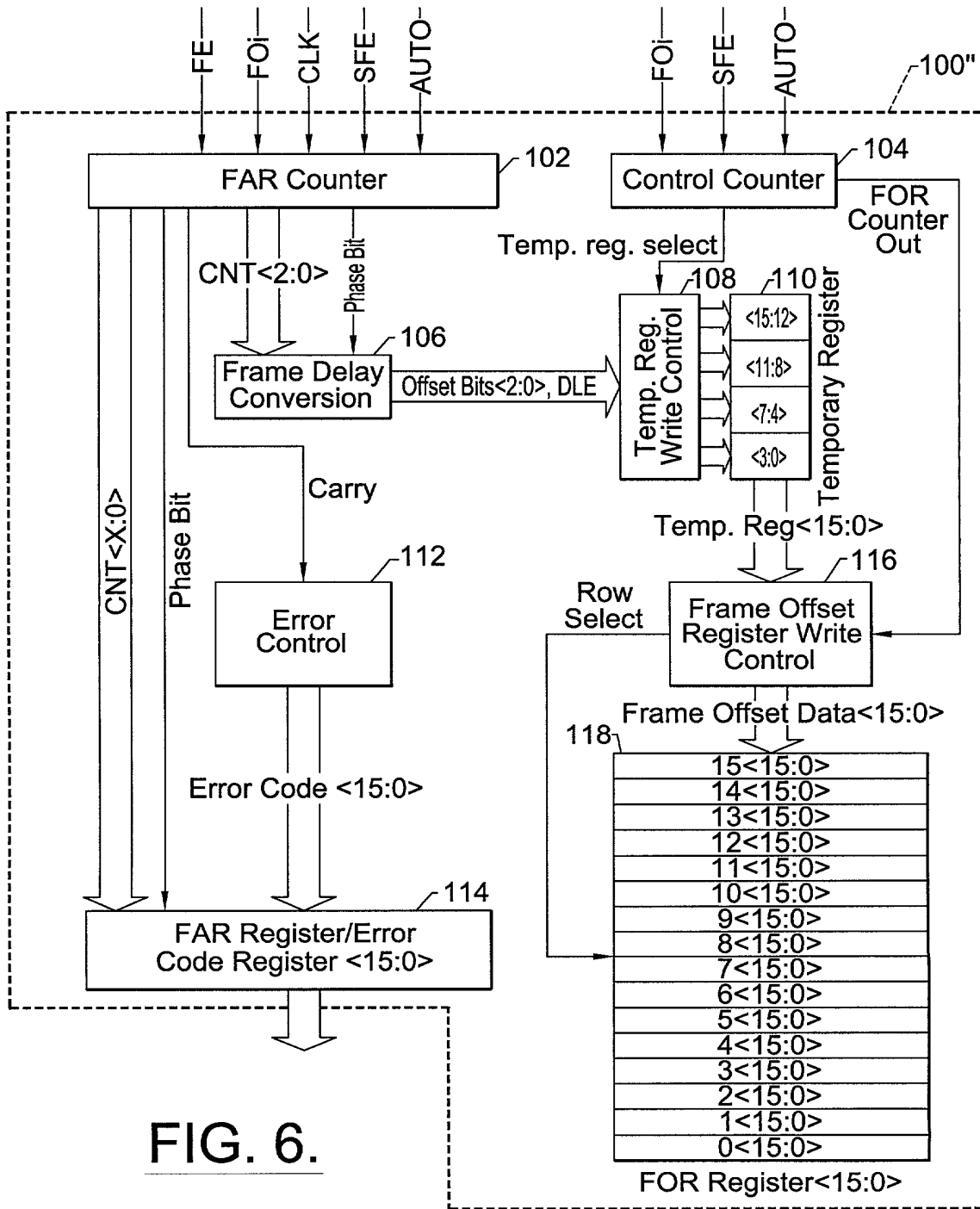


FIG. 4.





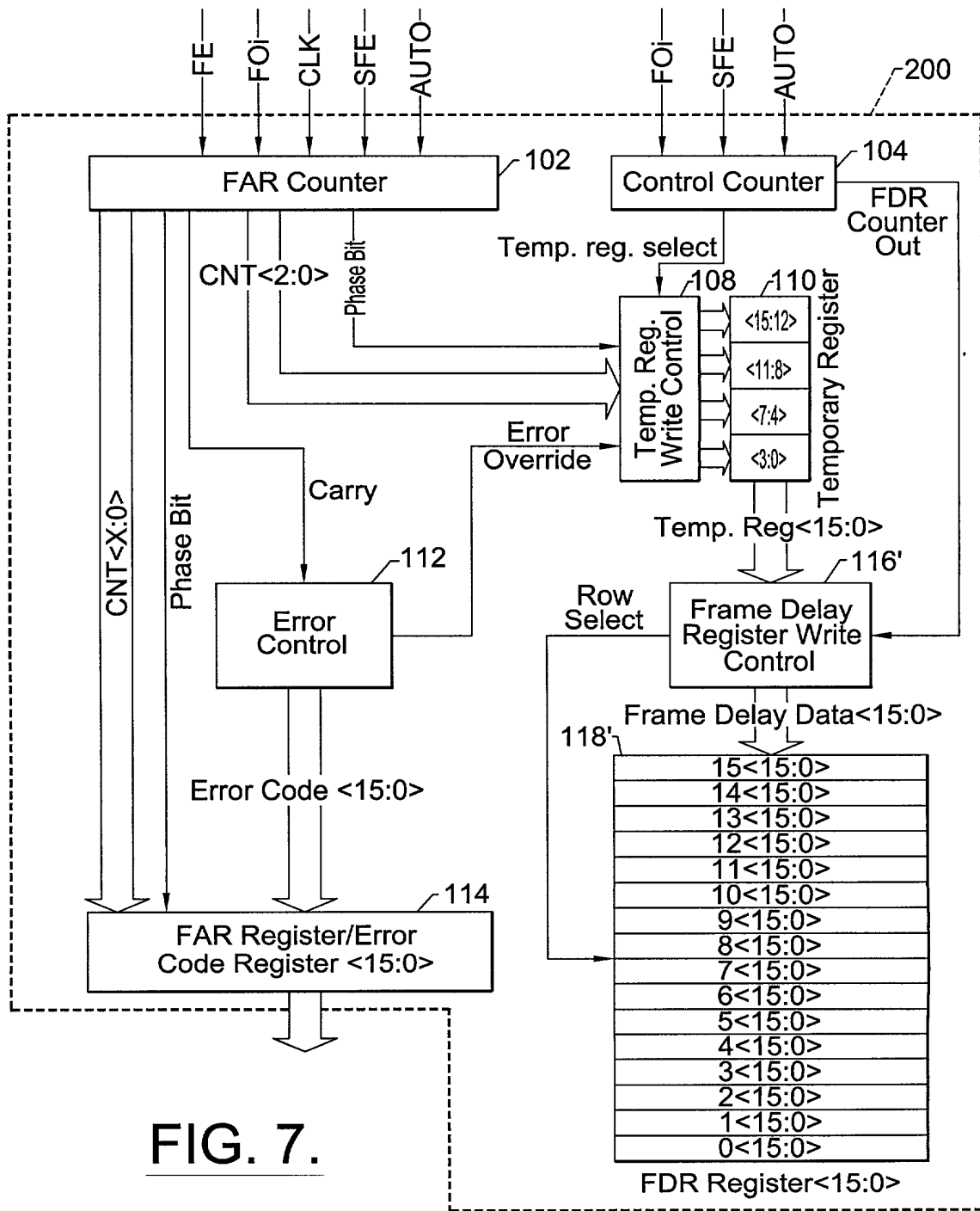


FIG. 7.

Input Stream Offset	Measurement Result from Frame Delay Bits						Corresponding Offset Bits			
	FD11	FD2	FD1	FD0	OFn2	OFn1	OFn0	DLEn		
No clock period shift (Default)	1	0	0	0	0	0	0	0		
+0.5 clock period shift	0	0	0	0	0	0	0	0		
+1.0 clock period shift	1	0	0	1	0	0	1	0		
+1.5 clock period shift	0	0	0	1	0	0	1	1		
+2.0 clock period shift	1	0	1	0	0	1	0	0		
+2.5 clock period shift	0	0	1	0	0	1	0	1		
+3.0 clock period shift	1	0	1	1	0	1	1	0		
+3.5 clock period shift	0	0	1	1	0	1	1	1		
+4.0 clock period shift	1	1	0	0	1	0	0	0		
+4.5 clock period shift	0	1	0	0	1	0	0	1		
+5.0 clock period shift	1	1	0	1	1	0	1	0		
+5.5 clock period shift	0	1	0	1	1	0	1	1		
+6.0 clock period shift	1	1	1	0	1	1	0	0		
+6.5 clock period shift	0	1	1	0	1	1	0	1		
+7.0 clock period shift	1	1	1	1	1	1	1	1		
+7.5 clock period shift (max)	0	1	1	1	1	1	1	1		

FIG. 8.